Page __1__ of __1__ Atty. Docket No. Serial No. U.S. Department of Commerce 10/055,088 HEUR-016 Patent and Trademark Office Information Disclosure Statement by Applicant Applicant: Arman Sagatelian et al. (Use several sheets if necessary) Filed: January 22, 2002 Group: 2858 **U.S. Patent Documents** Init. Document No. Date Name Class Subclass Filing Date 5,475,695 12/12/1995 Caywood et al. D 371 27 03/19/1993 **Foreign Documents** Translation Init. Document No. Date Country Class Subclass Yes No Other Documents (Including Author, Title, Date, Pertinent Pages, etc.) K. Tobin, "Automated Analysis for Rapid Defect Sourcing and Yield Learning", Future Fab International, 15 pages, Vol. 4, 1997 (no month). "Semiconductor Spatial Signature Analysis (SSA)", [Internet] http://wwwismv.ic.ornl.gov/projects/SSA.html, 6 pages, Revised March 31, 1999, printed 2/27/03 J. Segal et al., "The Value of Electrical Bitmap Results from Embedded Memory Arrays for Rapid Yield Learning", Digest of Papers, 2nd IEEE Latin American Test Workshop LATW2001, pp. 266-272, Feb. 2001.

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